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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 09/477,099
Filing Date: January 04, 2000
Appellant(s): DUNLAP ET AL.

Ryan S. Davidson
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 20 September 2005 appealing from the Office action mailed 13 December 2004.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

5365475	Matsumura et al.	11-1994
4777623	Shimazu et al.	10-1988

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1and 11 are rejected under 35 U.S.C. 102(b) as being anticipated by Matsumura et al. (U.S. patent No. 5,365,475).

As to claim 1, Matsumura et al. teaches a static random access memory (SRAM) device capable of storing a program that is accessible when said SRAM device is powered up, said SRAM device comprising a plurality of storage cells (see column 1, lines 15-19), each of said storage cells comprising:

a data latch having a first input/output (I/O) line and a second I/O line (see figure 3, *BL* and $\overline{BL}$), said data latch comprising:

a first inverter having an input coupled to said first I/O line and an output coupled to said second I/O line (see figure 3, NA); and

a second inverter having an input coupled to said second I/O line and an output coupled to said first I/O line (see figure 3, NB); and

a biasing circuit capable of forcing at least one of said first and second I/O lines to a known logic state when power is applied to said SRAM device, wherein said known logic state comprises a portion of said program (see figure 3, G_1, G_2, V_1, and V_2).

As to claim 11, Matsumura et al. teaches a data processor comprising a central processing unit (CPU) capable of executing a boot-up program when power is applied to said CPU (see figure 15), said CPU comprising:

a static random access memory (SRAM) device capable of storing said boot-up program, said SRAM device comprising a plurality of storage cells capable of storing bits of said boot-up program (see column 1, lines 15-19), each of said storage cells comprising:

a data latch having an input and an output (see figure 3, BL and $\overline{BL}$), said data latch comprising:

a first inverter having an input coupled to said first I/O line and an output coupled to said second I/O line (see figure 3, NA); and

a second inverter having an input coupled to said second I/O line and an output coupled to said first I/O line (see figure 3, NB); and

a biasing circuit capable of forcing at least one of said first and second I/O lines to a known logic state when power is applied to said SRAM device (see figure 3, G_1, G_2, V_1, and V_2), wherein said known logic state comprises a portion of said boot-up program (see column 11, lines 3-17).

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 10 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsumura et al. (U.S. patent No. 5,365,475) in view of Shimazu et al. (U.S. patent No. 4,777,623).

As to claims 10 and 20, Matsumura et al. does not teach wherein said biasing circuit comprises a grounding circuit selectively connected by a programmable connect to one of said first inverter output and said second inverter output, wherein said grounding circuit is temporarily enabled after power is applied to said SRAM device, thereby grounding one of said first inverter output and said second inverter output and forcing said second 1/O line to said known logic state.

Shimazu et al. teaches wherein said biasing circuit comprises a grounding circuit selectively connected by a programmable connect to one of said first inverter output and said second inverter output, wherein said grounding circuit is temporarily enabled after power is applied to said SRAM device, thereby grounding one of said first inverter output and said second inverter output and forcing said second 1/O line to said known logic state (see column 3, line 65 through column 4, line 14).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to have modified Matsumura et al. to include the teachings of Shimazu et al. because these teachings would allow the device to be set or reset in a more efficient manner (see Shimazu et al., column 1, lines 7-10).

(10) Response to Argument

A. Rejection of claim 10.

In response to the Appellant's arguments that "The Proposed Combination of the Matsumura and Shimazu References Fails to Disclose or Suggest the Grounding Circuit Features as Recited by Claim 10", the arguments have been fully considered but are not deemed persuasive. Figure 3 reference numbers 6a, 12, and 15 and column 3, line 65 through column 4, line 14 clearly discloses a grounding circuit connected by a transistor (programmable connect) to the output of inverter 3. The nMOS transistor attached to the ratio latch (semiconductor memory device) works in a way that when the voltage of 12 is raised to a certain point the "gate" of the transistor becomes saturated. At this point any voltage that is on line 6a can flow through the transistor 15 to the ground circuit. In this way the transistor marked as 15 in figure 3 works as a switch. Column 4, lines 11-14 states that the MOS transistor is able to work well enough "to pull down the [voltage] level of the input data line to "0" even when the input data is "1". This biasing circuit when used would set 6a to "0" making the output voltage at 8 be "1" based on the effects of the inverter.

Appellant's arguments state "Neither the relied-upon passage of the Shimazu reference nor any other passage of the Shimazu reference discloses or suggests a grounding circuit *selectively* connected *by a programmable select* to one of a first inverter output or a second inverter output as recited by claim 10." According to the circuit of figure 3 as discussed above and disclosed in column 3, line 65 through column 4, line 14, Shimazu teaches all the required limitations of Applellant's argument. The biasing device of Shimazu et al., discussed in the preceding paragraph, is attached to the output of inverter 3 and to the input of inverter 2 and is selectively connected to the grounding circuit. When the transistor (programmable select) is

turned on by raising the voltage on 12 the grounding circuit is temporarily enabled which then grounds the inverter 3's output. This places the output and input lines at known logic states.

A narrow interpretation of the claim language would require the programmable connect to switch back and fourth between the first inverter and the second inverter. This appears to be the interpretation that the Appellant has given the claim. The examiner tried unsuccessfully to point out in the Final Rejection that this was not the only interpretation that could be made of the claim. The claim limitation "one of said first inverter output and said second inverter output" makes it optional which output the "programmable connect" is connected to. Therefore, the grounding circuit only needs to be connected by a programmable connect to one of the outputs. This connection is made (selectively) whenever the programmable connect is "set" by raising the voltage of 12. This then "enables" the grounding circuit to interact with the SRAM device and forces the SRAM device into a known logic state.

The Appellant's arguments go on to state "the Shimazu reference provides no disclosure or suggestion that the transistor 15 is connected to the output of the inverter 3 by a programmable connect, so the Shimazu reference necessarily fails to disclose or suggest grounding circuit *selectively* connected by a *programmable connect* as recited in claim 10." The examiner does not interpret the transistor to be the grounding circuit. The transistor is interpreted to be the "programmable connect". By raising and lowering the voltage at 12 the output the programmable connect selectively connects the grounding circuit to the output of one of the inverters (in this case the output of inverter 3) as discussed above.

In response to the Appellant's arguments that "The Proposed Combination of the Matsumura and Shimazu References Fails to Disclose or Suggest Temporarily Enabling the Grounding Circuit as Recited by Claim 10", the arguments have been fully considered but are not deemed persuasive. The appellant's arguments state "neither the relied-upon passage of the Shimazu reference nor any other passage of the Shimazu reference provides any disclosure or suggestion related to temporarily enabling the transistor 15 after power is applied to the memory cell." The Shimazu reference clearly recites "the ratio latch 4 can be set by merely raising the output voltage of the power source 12". This setting enables the transistor in the sense that the path between the inverters and the ground is now open, like a switch. It is inherent that this setting is done after the power is provided to the memory cell. If there was no power provided to the memory cell before the voltage of 12 is raised, there would be no effect in the cell because in the powered off state the cell would be incapable of holding the set to state.

In response to Appellant's arguments that "The Combination of the Matsumura and Shimazu References is Improper Not only does the proposed combination of the Matsumura reference and the Shimazu reference fail to disclose or suggest numerous features of claim 10, there is no motivation to combine the teachings of the Matsumura reference and the Shimazu reference as proposed by the Final Rejection." The Matsumura et al. reference is used to disclosed a SRAM device that is initialized in a manner that the memory device contains a predetermined program after the initialization procedure is completed. The Matsumura et al. reference does this by supplying different voltages to the cell based on the state that the cell is desired to be in. For instance the cell disclosed in figure 5A is designed to be initialized into a

state of "0", and the cell disclosed in figure 5B is designed to be initialized into a state of "1" simply by changing G2 to "H" or high instead of "L" or low (ground). In order to put the cell into the different states the Matsumura et al. reference requires four supply lines that are normally set at two in the "H" or high position (V1 and V2) and two in the L or low position (G1 and G2). Depending on which of the four types of cells of the Matsumura et al. reference are being initialized, voltages on the various lines must be either switched from high to low or from low to high. This requires a switch for each of these voltage lines. Also when a voltage line is switched, only some of the cells will be initialized by the switch. For instance a change of voltage on V2 in figures 5A and 5B is not going to change the states of these cells at all. By changing the set device of Matsumura et al. from four voltage lines to the devices show in figures 3 and 4 reference numbers 12, 15, and 16 of the Shimazu et al. reference, the Matsumura et al. reference would only require three power lines one that is always high (V1 of Matsumura et al.), one that is always low (G1 of Matsumura et al.), and one that switches (12 of Shimazu et al.). If a "0" is desired to be set on BL in the Matsumura et al. reference (6 in Shimazu et al.), the device of figure 3 would be used. If a "1" is desired to be set the device of figure 4 would be used. This would initialize a program in memory similar to that of the Matsumura et al. reference, but would allow the entire SRAM device to be initialized with that program at the same time rather than only sections.

B. Rejection of claim 20.

In response to the Appellant's arguments that "The Proposed Combination of the Matsumura and Shimazu References Fails to Disclose or Suggest the Grounding Circuit Features

as Recited by Claim 20", the arguments have been fully considered but are not deemed persuasive. Figure 3 reference numbers 6a, 12, and 15 and column 3, line 65 through column 4, line 14 clearly discloses a grounding circuit connected by a transistor (programmable connect) to the output of inverter 3. The nMOS transistor attached to the ratio latch (semiconductor memory device) works in a way that when the voltage of 12 is raised to a certain point the "gate" of the transistor becomes saturated. At this point any voltage that is on line 6a can flow through the transistor 15 to the ground circuit. In this way the transistor marked as 15 in figure 3 works as a switch. Column 4, lines 11-14 states that the MOS transistor is able to work well enough "to pull down the [voltage] level of the input data line to "0" even when the input data is "1". This biasing circuit when used would set 6a to "0" making the output voltage at 8 be "1" based on the effects of the inverter.

Appellant's arguments state "Neither the relied-upon passage of the Shimazu reference nor any other passage of the Shimazu reference discloses or suggests a grounding circuit *selectively* connected *by a programmable select* to one of a first inverter output or a second inverter output as recited by claim 20." According to the circuit of figure 3 as discussed above and disclosed in column 3, line 65 through column 4, line 14, Shimazu teaches all the required limitations of Appellant's argument. The biasing device of Shimazu et al., discussed in the preceding paragraph, is attached to the output of inverter 3 and to the input of inverter 2 and is selectively connected to the grounding circuit. When the transistor (programmable select) is turned on by raising the voltage on 12 the grounding circuit is temporarily enabled which then grounds the inverter 3's output. This places the output and input lines at known logic states.

A narrow interpretation of the claim language would require the programmable connect to switch back and fourth between the first inverter and the second inverter. This appears to be the interpretation that the Appellant has given the claim. The examiner tried unsuccessfully to point out in the Final Rejection that this was not the only interpretation that could be made of the claim. The claim limitation "one of said first inverter output and said second inverter output" makes it optional which output the "programmable connect" is connected to. Therefore, the grounding circuit only needs to be connected by a programmable connect to one of the outputs. This connection is made (selectively) whenever the programmable connect is "set" by raising the voltage of 12. This then "enables" the grounding circuit to interact with the SRAM device and forces the SRAM device into a known logic state.

The Appellant's arguments go on to state "the Shimazu reference provides no disclosure or suggestion that the transistor 15 is connected to the output of the inverter 3 by a programmable connect, so the Shimazu reference necessarily fails to disclose or suggest grounding circuit *selectively* connected by a *programmable connect* as recited in claim 20." The examiner does not interpret the transistor to be the grounding circuit. The transistor is interpreted to be the "programmable connect". By raising and lowering the voltage at 12 the output the programmable connect selectively connects the grounding circuit to the output of one of the inverters (in this case the output of inverter 3) as discussed above.

In response to the Appellant's arguments that "The Proposed Combination of the Matsumura and Shimazu References Fails to Disclose or Suggest Temporarily Enabling the Grounding Circuit as Recited by Claim 20", the arguments have been fully considered but are

not deemed persuasive. The appellant's arguments state "neither the relied-upon passage of the Shimazu reference nor any other passage of the Shimazu reference provides any disclosure or suggestion related to temporarily enabling the transistor 15 after power is applied to the memory cell." The Shimazu reference clearly recites "the ratio latch 4 can be set by merely raising the output voltage of the power source 12". This setting enables the transistor in the sense that the path between the inverters and the ground is now open, like a switch. It is inherent that this setting is done after the power is provided to the memory cell. If there was no power provided to the memory cell before the voltage of 12 is raised, there would be no effect in the cell because in the powered off state the cell would be incapable of holding the set to state.

In response to Appellant's arguments that "The Proposed Combination of the Matsumura and Shimazu References Fails to Disclose or Suggest a CPU Comprising a SRAM Device", the arguments have been fully considered but are not deemed persuasive. The examiner notes the appellant's lack of argument towards the 35 U.S.C. 102(b) rejection of independent claim 11. Since Appellant did not appeal this claim, it is believed that Appellant feels that this rejection was properly made and that the limitations of claim 11 are fully anticipated by Matsumura et al. The limitation of "a CPU comprising a SRAM device" was first recited and rejected in this independent claim, and the primary Matsumura et al. reference is used in disclosing this feature as seen in the rejection above and as can bee seen figure 15 and the corresponding description in column 11. The secondary reference Shimazu et al. was added not to disclose the limitation of "a CPU comprising a SRAM device", but to disclose parts of the SRAM device claims in dependent claim 20 that were not completely anticipated by Matsumura et al.

Appellant's arguments are "The Final Rejection does not address this feature of claim 20." The examiner refutes this argument. As stated above the examiner rejected the limitation of "said CPU comprising: a static random access memory (SRAM)" with the Matsumura et al. reference when rejecting independent claim 11 on which dependent claim 20 depends. The 35 U.S.C. § 103(a) rejection of claim 20 relies on the rejection of claim 11 for these features.

The appellant's arguments go on to state "The Shimazu reference makes no mention of a CPU in any manner." The examiner acknowledges this and again refers to the Matsumura et al. reference for the rejection of this limitation.

The appellant's arguments also go on to state:

> "Figure 15 of the Matsumura reference discloses a microprocessor 104 having a CPU 105 and a program memory 106. However, as illustrated by Figure 15, the program memory 106 is separate from the CPU 105 and the related disclosure of the Matsumura reference provides no disclosure or suggestion that the program memory 106 can be implemented as part of the CPU 105."

In response the examiner reiterates the fact that the Appellant did not appeal independent claim 11, and that this shows that the Appellant believes this rejection is proper. Further, claim 11 recites that the CPU comprises the SRAM, but not where the SRAM is in relation to the CPU. Appellant is not stating that the SRAM is inside the CPU or how it is attached to the processing part of the CPU. Also the SRAM of Appellant's present invention is not doing the processing only holding the instructions to be processed and the results of that processing. Therefore the SRAM is not part of the processing part of the CPU (central processing unit), but somehow attached to it in order to perform as a memory device. As Matsumura et al. is used to disclose in the rejection of the conceded to rejection of claim 11.

In response to Appellant's arguments that "The Combination of the Matsumura and Shimazu References is Improper Not only does the proposed combination of the Matsumura reference and the Shimazu reference fail to disclose or suggest numerous features of claim 10, there is no motivation to combine the teachings of the Matsumura reference and the Shimazu reference as proposed by the Final Rejection." The Matsumura et al. reference is used to disclosed a SRAM device that is initialized in a manner that the memory device contains a predetermined program after the initialization procedure is completed. The Matsumura et al. reference does this by supplying different voltages to the cell based on the state that the cell is desired to be in. For instance the cell disclosed in figure 5A is designed to be initialized into a state of "0", and the cell disclosed in figure 5B is designed to be initialized into a state of "1" simply by changing G2 to "H" or high instead of "L" or low (ground). In order to put the cell into the different states the Matsumura et al. reference requires four supply lines that are normally set at two in the "H" or high position (V1 and V2) and two in the L or low position (G1 and G2). Depending on which of the four types of cells of the Matsumura et al. reference are being initialized, voltages on the various lines must be either switched from high to low or from low to high. This requires a switch for each of these voltage lines. Also when a voltage line is switched, only some of the cells will be initialized by the switch. For instance a change of voltage on V2 in figures 5A and 5B is not going to change the states of these cells at all. By changing the set device of Matsumura et al. from four voltage lines to the devices show in figures 3 and 4 reference numbers 12, 15, and 16 of the Shimazu et al. reference, the Matsumura et al. reference would only require three power lines one that is always high (V1 of Matsumura et al.), one that is always low (G1 of Matsumura et al.), and one that switches (12 of Shimazu et

al.). If a "0" is desired to be set on BL in the Matsumura et al. reference (6 in Shimazu et al.), the device of figure 3 would be used. If a "1" is desired to be set the device of figure 4 would be used. This would initialize a program in memory similar to that of the Matsumura et al. reference, but would allow the entire SRAM device to be initialized with that program at the same time rather than only sections.

C. Appellant's Conclusion

In response to Appellant's statements requesting reconsideration and entry of the "amendments submitted after the Final Rejection" in page 19 of the Appeal Brief. The examiner respectfully submits that this issue is not related to any of the grounds on appeal in the case, was previously decided and reviewed by a Special Programs Examiner, and therefore should not be considered by the board.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Jacob F. Betit
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Art Unit 2164

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Charles Rones
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An appeal conference was held on 22 November 2005, and it was agreed to proceed to the board of appeals.